

Guide to

Running SPICE Simulations using Mentor PADS 2009.1 DxDesigner & Hyperlynx Analog

Department of Electrical and Computer Engineering Spring 2010

(last revised 1/25/10)

Overview

This is a tutorial on how to get started with simulations using the Mentor PADS 2009.1 design tool. This tool can be used to simulate circuits using the DxDesigner schematic editor and the HyperLynx Analog SPICE simulator. This tool is also used to create printed circuit boards using DxDesigner schematic capture and PADS Layout. Information on creating printed circuit boards is covered in a different tutorial

Contents

1) Setting up the Directory Structure and Launching DxDesigner	3
2) Creating a Project for SPICE Simulation	4
3) Creating a Schematics for SPICE Simulation (Transient)	5
4) Running a SPICE Simulation (Transient)	9
5) Creating a Schematics for SPICE Simulation (AC)	15
6) Running a SPICE Simulation (AC)	16
7) Creating Subcircuits	18
8) Performing Parametric Sweeps	21

1) Setting up the Directory Structure and Launching DxDesigner

- A) Log onto the PC's in the digital lab on 6th Floor Cobleigh (COBH 601).
- B) Setup your directory structure (if your first time using DxDesigner)

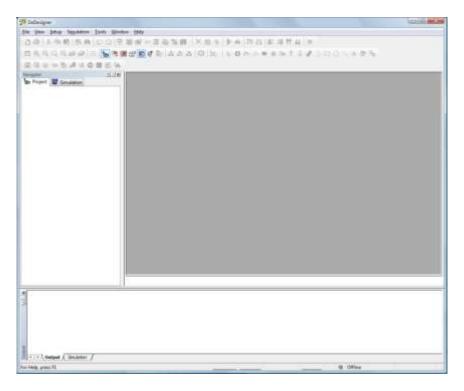
- DxDesigner uses *Projects* to hold all of your schematics and simulation results. One *Project* may contain numerous schematics and simulation results in addition to other more advanced items. When you create a *Project* in DxDesgner, you will enter a project name and it will create a new folder with the name you provided.

- to keep things organized, create a folder called "PADS_Projects" in which all of your project subfolders will be created in. Subfolders will be created by DxDesigner when you create projects within the tool.

C) Start DxDesigner using:

[Start] – Programs – Mentor Graphics SSD - Design Entry – DxDesigner.

You should see the following window appear:



NOTE: Multiple versions of PADS can be installed on PC simultaneously. Check that the version of DxDesigner is **PADS2009.1** by performing:

Menu: Help - About

D) Enable the HyperLynx Analog Simulator by performing:

Menu: Setup - Settings

- On the left side of the window, highlight "Licensing".

- Now check the "HyperLynx Analog" box on the right side window to enable SPICE simulations in this project.

Settings	۲ کار
Clicensing Schematic Editor Schematic Editor Schematic Editor Schematic Editor New Sheets Text Nets Interconnectivity Table Sice and Dice Properties Navigator Symbols Nets and Buses Display Objects Font Mappings DxDesigner Diagnostics Cross Probing HDL Simulation Run on Startup Advanced	Check out all available features DxDataBook database support Hyperlynx Analog DxRFEngineer Select All OK Apply Cancel Help

- Click "OK"

2) Creating a Project for SPICE Simulation

A) Create a New Project

Menu: File - New Project

- On the left side of the window, click on "HLA Library" to enable SPICE libraries in this project.

- In the "Name" field, enter a descriptive name for your project such as "EE461_HW_and_Labs_SPICE". Notice that putting "_SPICE" will make it easy to see that this project is for SPICE simulations. Remember, multiple schematics and simulations can be created within this project.

- In the "Location" field, browse to your "PADS_Projects" directory.

- In the "Layout Tools" field, select "PADS9.0

Project Templates: mediat	18.A Genev			
default HSA Otto Library Defaulterers	the spectral less properties. Diffe	plate belongs to the Twells wit flaves are not compared back brow, why, the flaves		ed its area and symbol
	Leader	C Laws Book 1.14	Mener(2_Warting EH25_Proper	Checking and the
	Elline terrore s	ierve Configuration Mana	or	
	Gener Name			
	LayoutTool	PA059-0	•	Advance
				Canad

- Click "OK"

3) Creating a Schematics for SPICE Simulation (Transient)

A) Create a New Schematic

Menu: File - New - Schematic

- Under the "Project" tab, you will now see a "Designs" folder. Expand this folder and the "Design1" folder beneath it.

- You will see a new schematic called "Schematic1". Rename this schematic to something descriptive. Each schematic can only contain one SPICE circuit. Name each schematic that you create with a descriptive name not only indicating what the circuit it, but also what type of simulation it is performing. Affix a suffix such as "_TRAN", "_AC", or "_DC" to indicate what time of simulation the circuit is to be used for.

For this example, change the name from "Schematic1" to "Lab1a_RC_Circuit_Step_TRAN"

NOTE: This tool automatically saves each time you perform an action. As a result you do not need to manually save your design.

B) Make the Symbol Libraries Visible

Menu: View - DxDatabook

- This puts a new window at the bottom of DxDesigner that contains all of the SPICE parts you will be able to use in your schematic.

C) Make the Properties window visible

Menu: View - Properties

- This puts a properties window on the right of the DxDesigner window. This window will allow you to alter the properties of the components you enter in your schematic.

	And Rowan Security				PET-116	6, 100 pr	1,000,020	141-14	ata a c	est he	TRACLE			_			labilit ge
	NICO PES					a 15	101		d and								- 10
	I LAND									0.0		1.6					
STRENCE.		100 m 10		1.25	- 100		-			-	0.000						
	114	_	_												_	Durbe	
Pepet Excedence																Property	Value
E Hatt (Hit) and Lanc D Designs	PICE .															15pm	- 1
- Cesieni																Drawing Sea Orientation	# Lardad
E G Leta (C,C)	Stoal, Sap_TRAN															1940	17,000
b Both																Hegh	11.000
															_	•	
	15	Bieth RC															

D) Enter a Schematic (A simple RC Circuit)

- Enter a voltage source

- In the DxDataBook window at the bottom of the DxDesigner window, click on the "CL View" tab. This will show the available symbol libraries for simulation.

- Scroll down to the "SpicePrimative" library and expand it by clicking on the + sign.

- Scroll down in the SpicePrimative library until you see the "v_pulse" symbol. Click on it and you will see its symbol show up in the preview panel (bottom right).

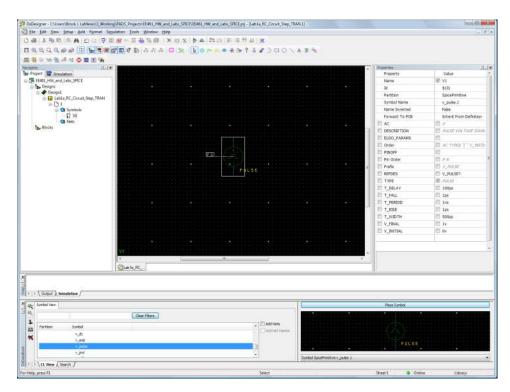
- Click on the "Place Symbol" button above the preview panel. The component will attach to your mouse. Click in the schematic sheet to place the component.

- Right Click to end the placement command.

- Click on the v_pulse component and set the following parameters in the parameter window (right side of window)

Name	= V1
T_DELAY	= 100ps
T_FALL	= 1ps
T_PERIOD	= 1ns
T_RISE	= 1ps
T_WIDTH	= 500ps
V_FINAL	= 1v
V_INITIAL	= 0v

NOTE: If you check the box for the individual parameter, it will display on the schematic.



- Enter a resistor

- In the SpicePrimative library, highlight the "r" symbol and click "Place Symbol" in the symbol preview pane.

- Click in the schematic window to place the component then right click to end.

- In the parameter pane, set the resistor parameters to:

Name	= R1
Value	= 50

- Enter a capacitor

- In the SpicePrimative library, highlight the "c" symbol and click "Place Symbol" in the symbol preview pane.

- Click in the schematic window to place the component and then right click to end.

- In the parameter pane, set the resistor parameters to:

Name	= C1
Value	= 1pF

NOTE: You can rotate the symbol by highlighting it, then right clicking and selecting "Rotate"

- Enter a GND connection

- Click on the "Ground" icon in the Add toolbar along the top of the screen. When you click on the this icon it will expand into a dropdown menu, select "builtin:gnd.1".

- Place the ground symbol in the schematic and right click to end.

- Position the components into a an easy-to-connect circuit formation. You can move components by clicking and holding a component, then moving.

ie Lidt View Setup Add Format	Sigulation Look Mindow Help			(RAN.1)		
GIBBBBB BB DOD						(+ <i>#</i>)
	医偏血管管脊髓 火车					
q Q Q Q 🖉 📾 🐂 🐂 💐 🕼	10 4 5 4 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	REPAREN	311 2 2 0 0 V	A # 34		
🗑 🔍 😘 🖻 🖉 🕫 🥥 🔳 🖄 😘						
nin	1× 000000000000 ×				Atsartive :	(111)
Proyect 📅 Servulation					Property	Value
EE4EL>W_and_Labs_SPICE					Name	1
in I Design					Drawing Size Orientation	B Landscape
E Labla_RC_Circuit_Step_TRAN					With	17.000 in
e 🗅 1 e 😋 Symbols					Height	12.000 m
\$T \$1113					mage	Transfer at
Ū \$1117						
🕄 VI.						
Tay Blocks	100200000000000000000000000000000000000	PULSE			the second s	
	CONTRACTOR STATES					
					2	
			GRO			
	E COMPANY STREET			= (1,1) = (1,1,1) = (1,1,1) = (-1,1)	* 11	
	1.	10 JP.			•	
	Salab 1a_RC					

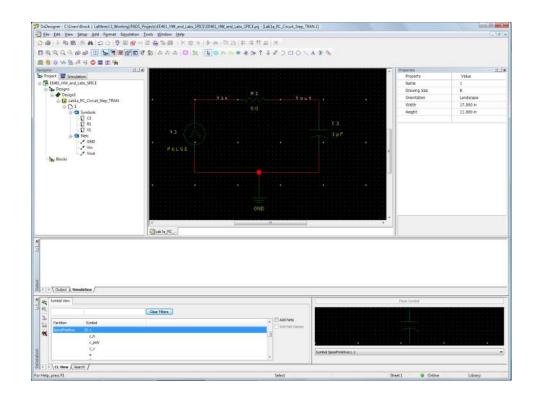
- Add nets to the circuit

```
Menu: Add - Net (or press the "n" button)
```

- You enter nets by clicking-and-holding. Start the net at the pin of a device and drag it to the destination pin.

- Wire up the entire circuit

- Name the nets of the circuit
 - Click on the net between V1 and R1. In the parameters window, enter: Vin
 - Click on the net between V1 and R1. In the parameters window, enter: Vout



4) Running a SPICE Simulation (Transient)

A) Netlist the Design

```
Menu: Simulation - Netlist (or click the "Netlist Design" icon)
```

- In the menu that appears, you can select the simulation options. Most of the time you can accept the defaults. Ensure that the Target Simulator is set to HyperLynx Analog

- Click "OK"

- You will see the status of the netlist appear in the Output panel. This is where you will be notified of any netlisting errors.

- The result of the netlist operation was the creation of a TestBench and a SPICE text model of your circuit.

- Click on the "Simulation" tab in the Navigator panel. Expand the TestBenches folder. You will see a testbench named "Lab1a_RC_Circuit_Step_TRAN". Expand the "Files" and "Spice Files" folders beneath it. You will now see the text SPICE netlist of your circuit. Click on it and view the results. This file will be the first place to look if you receive netlist errors.

A STRATE AND A CONTRACTOR OF A DATA AND AND AND AND AND AND AND AND AND AN	Congroup (and a constant of the sector (Constant) along ROY		Cold with
] for hat you have figuress from Heater	*		
(本)未完時(水井)の(中国第一	S 볼 5월 (X B X I) A (5) () 대부상 H		
BRRDROD IN STREET	Blaza D(blenn+ehti#3005aph)		
#NEOFFERS			
		(Souther	
-Frant Struktor	* Anniert Sable MC Circuit Dier TAAP	Popety -	Take
Tanuartum, Analysis and Recards (\$285), Hill, and Lake.	* Mentor Singhios Rivelist Crested with Versian 6.3.14	15/14	4
· A Setlerches	* File created fun Jak 24 15:16:54 1515 * Dolfile	Orawing Spa	
W Lakis AC, Dook Ster Team (a Chile) in 4 Feet	* Confightle: CriMentarGraphics #BLADDIE.119. CHEDDIDU BDBELatenderd waring of	Diet/attack	Gentionex
- # VHDLFilm	* Options :est -k -S -Schlamonstraphing #Add2009.118.184401.000 mome	19465	17.000 #
 B Variag First B Specifies 	1 Isreli (Heght	12.008 =
Biotics/Const.Ney,1998ap Biotecnet Ney Biotics Biotic	<pre>v_primitive via 0 at 0 arises (for tr 100pe type los 500pe ine) El via via via 00 Cl Post 0 log v_a discissary 1 * Good - 2 * Good - 2 * Good - 3 * Good - 3 * Global 3 * Global 3 * Global - 3 * * * * * * * * * * * * * * * * * * *</pre>		
	Para Para Para Para Para Para Para Para		
	Gaster David		
	C:10ee501nck 3: LaMerei (J. Working/F405_Project/)E441_WV, and Lalm_F4021npm/incodejan.kg http://doi.org/10.1040/5500_H6ME/wv/wH32bel.dom_wapce.msgv -h -l -KC?(Mentor/caphor_P405) TBBA	NOR UN IRADS (SUD.)	O'Elstandardissipice cly
+(+)(0.00) Soulation/			
Reg Symbol New		Pare Serial	
Res Sector free	(ar%s)	Pare Simble	
+ (+ \ ()(()) \ Socialities /	g Eather	Pare Serial	
Ar Selar Hen Sa Partier Smith		Part Setol	
An Selection Sel	g Eather	Pare Series	
State State	g Eather	The Set	
An Serier Inn	g Eather	Plac Setol	
e Seletite S Seletite S Seletite		Peet Secol	
Real Factor Sold		Per Sinol	

B) Simulate the Design

- In the Simulation tab of the Navigator panel, right click on the "Lab1a_RC_Circuit_Step_TRAN" testbench and select "Simulate"

Note: The first time you enter a circuit, you need to netlist the schematic in order to create the TestBench. From then on, you can just perform a simulation command and it will automatically netlist the circuit.

- the "Simulation Control" window appears. This is where you will setup the SPICE simulation.

- On the left side of the window, highlight "Simulations". On the right side of the window you will enter the name of the file where the simulation information will be contained. Give this the same name as your schematic (i.e., Lab1a_RC_Circuit_Step_TRAN"). The name you give is arbitrary, but giving it

the same name as your schematic will make it easier to find your results later.

- On the left side of the window, highlight "Time-Domain Analysis". On the right side, enter the following:

Enable	= checked	
Start Time	= 0s	
End Time	= 10ns	
Tmax	= 1 ps	(this is the simulation step size)
Printing Time Interv	al = 1ps	

- By default, the simulator will record all voltages and currents for every node in the circuit. If you want to only record specific information, you can set this up by

highlighting "Results:time-Domain Waveforms" on the left and then checking the nodes you wish to record. This becomes important when you are running larger circuits and want to reduce simulation time.

DC Analysis	Contraction of the local division of the loc			
Time-Domain Analysis Frequency Analysis	-			
Philli Run Hultiple Seeap	Settings			
Parametric Sweep Temperature Sweep	Start Tree	4	Calde sites	True Item
Statutical Analysis Optimizer	End Tave	1004	Ipp image	Treas
Sesuits Operating Point Values	Posting Taxe 3 views	tps		
 Time-Domain Mayeforts FFT Waveforts 	Advanced Softrage			
DC Sinteg Waterforms	Contract free parameters in	The second second		
Requescy Waveforms Distribution Results	Connect Inter-Indexed	Total and the second se		
E-perivent Pile Advenced	Prover Designation			
	- then Int			
	musc			
	-			

- Click the "Simulate" button.

C) View the Results

- A new window will appear called "EZwave", click on this to bring it to the front. On the left of this window you will have a "Waveform List" which gives all of the simulation database results. You will see the "Lab1a_RC_Circuit_Step_TRAN" results. Expand this folder. Under this folder you will see the simulation type results (i.e., TRAN). Highlight TRAN.

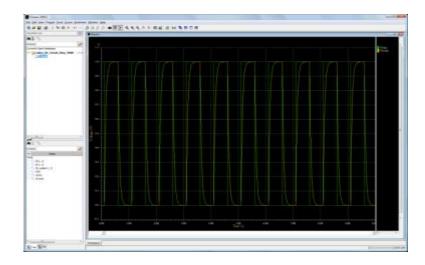
- By highlighting TRAN, you will now see all of the available simulation results that can be displayed. You can add waveforms to the display panel either by double clicking or dragging and dropping.

- Add the V(vin) and V(Vout) waveforms to the same plot.

NOTE: If you double click on the net names, it will create new plots for each net. You can drag/drop the net names on the right side of the plot onto a different plot to get both simulations results on the same graph.

- You can turn on the grid by performing:

Menu: View - Grid (or by clicking on the Grid icon)



D) Take Measurements on the Waveform

- EZwave has built in measurement capabilities. You can measure the risetime of the output waveform automatically using the "Measurement Tool"

Menu: Tools - Measurement Tool

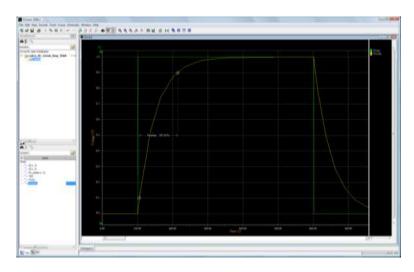
- When the "Measurement Tool" window appears, in the "Measurement" field, click on the pre-defined measurement buttons (defaulted to Average). This will give a drop-down of available measurements. Select "Risetime.

- Now highligh the V(vout) waveform in the main EZwave window. In the "Source Waveform", field of the "Measurement Tool" window, click the "Add Selected Waveform" button.

- You can set the definitions for the risetime measurement but it will default to 10% to 90%. Click "Apply"

ent : Al Types · Risetime	
Waveform(a)	
(vout)	0
rment Setup	
Topine : CAutomatic> • 🕅	
Sauline : <automatic> +</automatic>	
r/Upper: 20% - 90% - 🕅	
evels are Relative to the Topkne and Baseline	
ement Results	
notate Waveform(s) with Measurement Results	
t New Waveform of 'Risetime' vs 'Time'	
acurement to : Entire Waveform	
tenove Al Previous "Risetme" Results	

- The measurement will appear on the EZwave waveform. You can zoom in on the measurement by clicking and dragging in the vertical direction on the plot to zoom in on the voltage axis and horizontally on the time axis.



- The risetime should be ~110ps (i.e., 2.2τ or 2.2RC)
- You can close the window

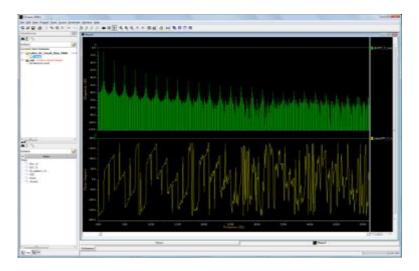
E) Perform an FFT of the Waveforms

- In the EZwave window, perform:

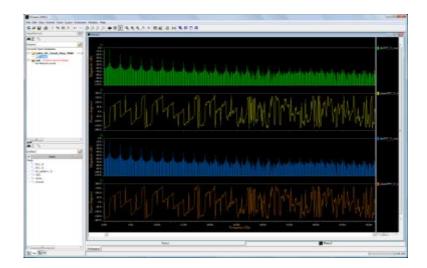
Menu: Tools - FFT

- Select the V(Vin) waveform as the "Source Waveform"

- Except the defaults and click "Apply"



- Now perform an FFT on V(vout) using the same procedure.



- You can delete waveforms by highlighting them and clicking the "Delete" button. Delete the phase for both waveforms.

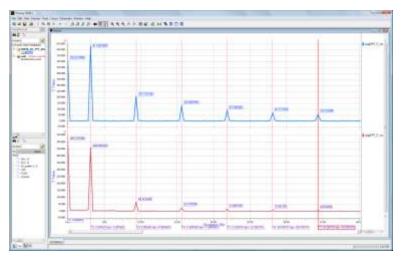
- If you click on the "Advanced" button in the FFT Tool window, you can select "Magnitude" instead of dB and Phase.

- If you perform:

Menu: Cursor – Add

you can continually add cursors.

- Within the EZWave view, you can change the background to white using:



Menu: Format – Color Scheme – White Background

- Close the EZwave viewer. You can save your results, but it is often unnecessary for small circuits because they can be recreated quickly. All of your results are stored in the *.cmd file setup by the Simulation Control window you configured earlier.

5) Creating a Schematics for SPICE Simulation (AC)

A) Create a New Schematic

Menu: File - New - Schematic

- This will be the second schematic in your project. When you create the schematic it will appear under "Blocks".

- Rename this schematic to "Lab1b_RC_Circuit_Step_AC"

- B) Enter a Schematic (A simple RC Circuit)
 - Enter a voltage source

- In the "SpicePrimative" library, place the "v" symbol and enter the following parameters:

Name
$$=$$
 V1
AC $=$ 1v

- Enter a resistor

- In the SpicePrimative library, place the "r" symbol and enter the following parameters:

Name
$$= R1$$

Value $= 50$

- Enter a capacitor

- In the SpicePrimative library, place the "r" symbol and enter the following parameters:

Name = C1Value = 1pF

- Enter a GND connection

- Click on the "Ground" icon in the Add toolbar and place "builtin:gnd.1".

- Add nets to the circuit

Menu: Add - Net (or press the "n" button)

- Wire up the entire circuit and name the input net "Vin" and the output net "Vout"

Billinger - Citierthus Latterill, Noting R	and Property and Jan. 2012 (1983) (19	Line SHEPP - Links HC, Deve ACH			Cold MO
its in the part of the sea south	nar Josh Hindow 1940				1.00
0414555420955		(新学生) (1)			
TSSC & d III N THE	DVB AAA O'S BOA	*************	1.2.3		
GSSAS440ELA	and an other states of the states of		5 (F		
				-1-	
The Project III Southeast	tite -			Property	Value
in the little way have with				Serv.	1
- b Despit				Drawing Say	
and the second				Owblar	Landicipe
⇒ B Lola, K, Smit, Say, 7844				web	17.000 m
E Lalb, R. Grad, AC				megt	21.800 in
eft:	THE COOL OF THE COURSE				
in 🔁 Tyerinyis	¥.a.				
1 a					
D at D at	and the second s				
	and a second second			1	
26 V					
1 to					
" test					
				10	
				8	
				10	
				-	
	1	* *			
	Bab S.			-	
and of AC Section Commands"					
+(+)(0.tp.t) Sediction /					
Revealed Here			6	Pice Limbel	1
4. pt	Detter				
2	And a state of the	CENtes			
Pertion Synkel					
		all for the second			
*		15			
58.		- 18	Denixi Salafenti en 2-		
+ (+)(0. New (Seem)					
diants allefed		later.		et @ Onie	Library 1

6) Running a SPICE Simulation (AC)

A) Netlist the Design

```
Menu: Simulation - Netlist
```

(or click the "Netlist Design" icon)

- In the window that appears, ensure that the Target Simulator is set to HyperLynx Analog. It will prompt you asking whether to make this design ACTIVE. Click "Yes". DxDesigner will only simulate the ACTIVE testbench.

- Click "OK"

B) Simulate the Design

- In the Simulation tab of the Navigator panel, right click on the "Lab1b_RC_Circuit_AC" testbench and select "Simulate"

- In the "Simulation Control" window, highlight "Simulations" on the left side of the window and enter "Lab1b_RC_Circuit_AC" for the experiment name.

- On the left side of the window, highlight "Frequency Analysis". On the right side, enter the following:

Enable	= checked
Frequency Start	= 1k
Frequency Stop	= 100G
Number of points	= 100
Variation type =	Decade

Dimutatione DC Analyste	Constanting of the local diversion of the loc	101 (U	
Time-Domain Analysis Frequency Analysis	Real		
Pluts Run (ii: Muttale Sudep)	Settrop		
Parameter (weep Texperitare (weep	Prequency Start.	10	
Statestical Analysis Continion	Pressency Stop	LING	
Results Operating Priorit Villues	Number of Points	200	
Time Donam Waveform	Variation Type:	Decode (1), *	
DC Sweep Waveforms Pressures Waveforms	Advanced Analysis		
III Commastori Resulta Experiment Pie	E Senativity	(Small)	
Advanced	Distortor	(Select)	
	These	Setup	
	-6		

- Click the "Simulate" button.

C) View the Results

- The "EZwave" window will appear, click on this to bring it to the front. On the left of this window in the "Waveform List", expand "Lab1b_RC_Circuit_AC" and highlight "AC"

- Add V(Vout) waveforms to the same plot.
- You can delete the phase portion of the plot.

- On the right of the waveform, double click on the dB(V(vout)) expression. Edit the expression to be db(V(vout)/V(vin)) in order to get the ratio of Vout to Vin.

- Turn on the grid by performing:

Menu: View - Grid

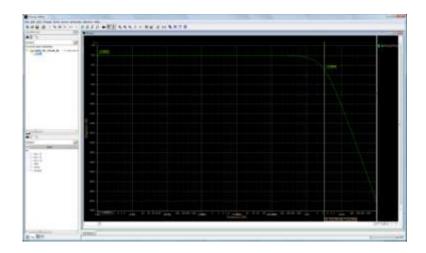
- Add two cursors to the waveform:

- select the waveform
- Perform

Menu: Cursor - Add to add the first cursor

Menu: Cursor - Add to add the second

- Grab the second cursor and move it over to the frequency at which the response falls to -3dB



- the -3dB frequency should occur at ~3.1GHz. This corresponds to $1/(2\pi RC)$.

7) Creating Subcircuits

A) Create a new schematic

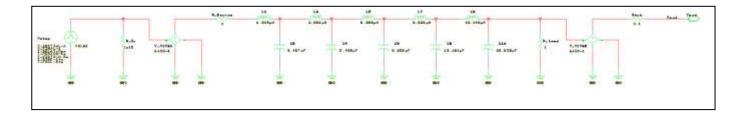
Menu: File - New - Schematic

- Rename the Subcircuit something descriptive. Consider naming all of your schematics that will used as a Subcircuit for another circuit something with a prefix "SUBCKT_". That way it will be obvious which schematics are subcircuits. NOTE: You CANNOT start a Subcircuit with a number, it has to be a letter.

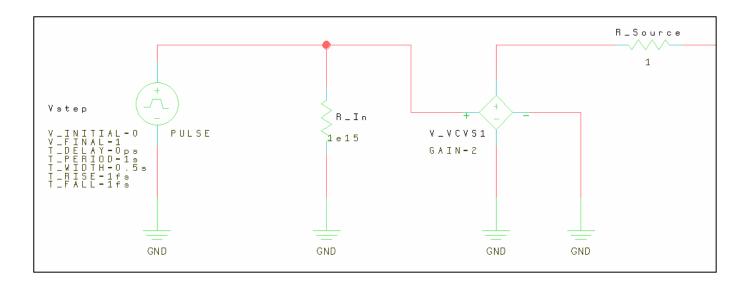
- For this example, we will make a 35ps Gaussian step source. Call the schematic "SUBCKT_Gaussian_Step_35ps"

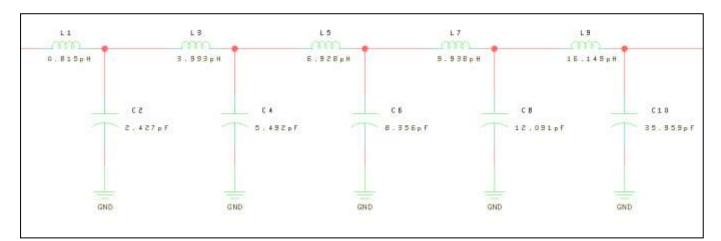
B) Enter a schematic

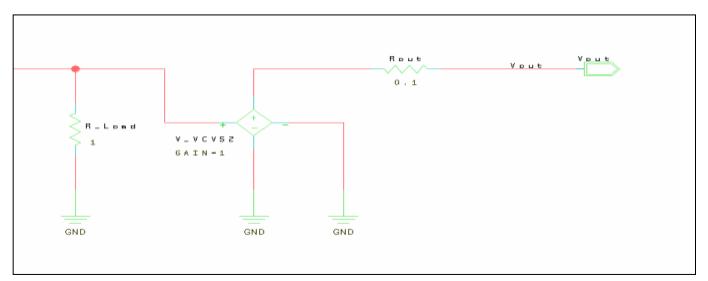
- Enter the following circuit to implement a Gaussian step:



(see below for zoom of the three main sections of this circuit)







- For the output of this circuit, place a **Port** by doing:

Menu: Add – Port – Out – builtin:port_hier_o.1

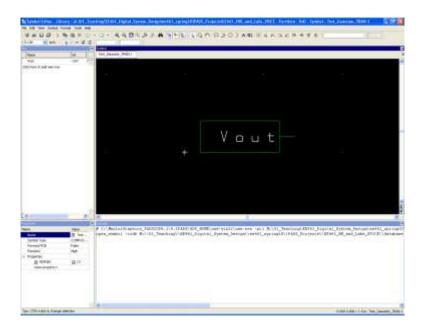
- Name the Port "Vout". This name will appear on the symbol

C) Create a Symbol

Menu: Tools – Generate Symbol

- Click "OK" on the Generate Symbol dialog to accept the default name. The name of the symbol will be the same as the schematic

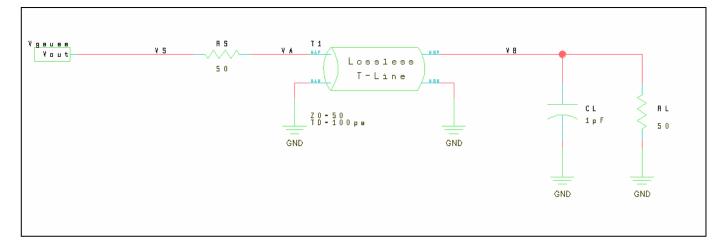
- The "Symbol Editor" window will appear with a symbol that was automatically created for you. You can edit the symbol in this window if you want to rearrange the pin locations, add text, or resize the symbol. If you are satisfied, save and exit this window.



- The symbol you just created will be placed in your [local symbols] library and can be placed in a higher level schematic just like any other part.

8) Performing Parametric Sweeps

A) Enter the following Schematic



- We are now going to run a parametric sweep on CL sweeping its value from 1pF to 3pF in steps of 1pF.
- B) Setup the Simulation

- Netlist and start the simulation as in a typical simulation.

- Setup the Transient Analysis to run from 0 to 1ns in steps of 1ps in the Simulation Control window.

- C) Setup the Parametric Sweep
 - On the left side of the Simulation Control window, highlight

Multi Run - Multiple Sweep - Parametric Sweep

- Setup the following:

Type = Dev Name = Broy Parametric	
Step Type	= Linear
Sweep Start	= 3p
Sweep Stop	= 3p
No of Points	= 3

- Click "ADD"

- Click "Simulate"

Stubions	E CONTRACTOR DE		
DC Analysis Tana-Consult Analysis Frequency Analysis	Text Parameter		
- Multi Run	Type: Device et		
Philiple Sweep Parametric Sweep	Nerrer Q. Brinner		
Temperature Sweep	Porander value		
Statistical Analysis Optimizer			
PessRs			
Operating Point Values Time-Operating WaveFores	Oters		
FF7 Wavefortee	Step Type Unice 🗶 and the main type	- Terr	
DC Sweep Waveforms Pressency Waveforms	Seeap Dart Ip		
# Optimization Results	Sweep Stage 30		
Experiment File Advanced	Number of Points 3		
	Parameteric Sweep Constants		
		A31	
		Dalates	

- This will run three separate simulations that can then be plotted on top of each other in EZWave

- In EZWave, plot all three waveforms for Va. You can adjust the color and line width of each waveform

