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High Speed Digital Systems Require Advanced Probing Techniques for Logic Analyzer Debug

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Abstract

Digital systems are turning out designs with faster edge speeds, double data rate clocking, and differential signaling to enable such systems to run faster than before. Adopting these techniques requires new considerations in circuit design, board layout, and system validation. Signal integrity is a term used to describe the quality of the signals in the system. If careful consideration is not given to the quality of the signals in the system, the design may fail to function properly. Signal integrity is emerging in the vocabulary of digital designers, a main focus of the definition, design, and debug of circuits and pc boards.

Logic Analysis provides validation at the system level of complicated digital designs such as memory systems. As memory architectures advance, state machines are being implemented on the IC to manage information exchange (DDR). In this new era, the success of the system relies as much on the system's timing and signal integrity as the performance of the silicon itself. In this new era, designers are expanding their testing off of the wafer and onto the PCB to verify the silicon in its destined environment.

When probing high-speed digital signals with a logic analyzer, the designer must take the electrical characteristics of the probe into consideration as well as the system itself. Designers are learning that not only do the electrical characteristics of the probe matter, but also the electrical characteristics of the methods used to connect to the probe. The connection to the probe is part of the circuit. The connection to the circuit is part of the probe. The design must account for probing *and* techniques when evaluating the effect of logic analyzer probing on the system's signal integrity.

This paper presents a variety of the most common signal integrity problems encountered when using logic analysis to verify high-speed digital systems. It will then describe in detail the most common design consideration when probing a digital system known as "stub-probing". Modern logic analysis probing solutions are then presented with an emphasis on memory validation at the system level.

Author(s) Biography

Brock J. LaMeres received his BSEE from Montana State University in 1998 and his MSEE from the University of Colorado in 2001. He is currently a hardware design engineer for Agilent Technologies in Colorado Springs, CO where he designs logic analyzer probes. He is also a part-time instructor at the University of Colorado in Colorado Springs in the area of microprocessor systems. His research interests are modeling and characterization of transport systems and high-speed digital design. LaMeres is a registered Professional Engineer in the State of Colorado.

I. Introduction

Over the past decade, signal integrity has come to the forefront of the communications industry. Faster data transfer rates and snappier rise times are causing engineers to incorporate microware design techniques into digital systems realized on a printed circuit board (PCB). This is especially apparent in modern memory system design. As transfer rates increase, engineers are adopting architectural changes such as source synchronous data and double-data-rate (DDR) clocking to overcome these signal integrity barriers. With IC processes progressing at or above Moore's Law, the bottleneck of these systems is now occurring on the PCB. This means engineers must include testability at the system level into their project schedules to ensure the overall success of their products. The tool of choice for digital system designers wanting to observe large signal counts is the Logic Analyzer.

While system level test provides a higher level of insight into communication problems, probing these systems has its own set of challenges. The same set of signal integrity rules that were followed to implement the system-under-test must also be considered when connecting a logic analyzer probe. The probe itself will introduce reflections and rise-time roll-off within the system. And conversely, the location of the probe and technique used to connect the probe will affect the performance of the logic analyzer.

This paper discusses the effect of the probe on the system and the effect of the system on the probe. It will examine in brief the load model of the logic analyzer probe and discuss quick methods for estimating the degradation due to the probe. It will then explain the effect of the location of the probe. It will then cover in depth one of the most common questions that designers have "how far away can the probe be and still operate?". Finally modern logic analyzer probing solutions are presented with an emphasis on memory system probing.

II. Load Model of the Logic Analyzer Probe

The goal of any type of probe is to present the smallest electrical load to the system as possible. If the probe alters the performance of the system too drastically, the probe does not help the designer validate his system because the cause of failure may be entirely due to the probe. The isolation of the failure is important to effective validation of a failure. Thus, the designer must be able to predict the effect of the probe on the system whether it is negligible or dominate.

The most accurate way to predict the performance of a probed system is to include a probe load model in the system simulations. Logic analyzer vendors provide RLC circuits that model their probe loads up to a pre-defined frequency (usually 6 GHz). Simulations not only provide the most accurate model of the probe's affect, they provide a way to alter variables and monitor each variable's effect. These variables include probe location on the transmission line, and/or probe stub length from the transmission line to the probe tip.

In general, a logic analyzer probe will look as follows:

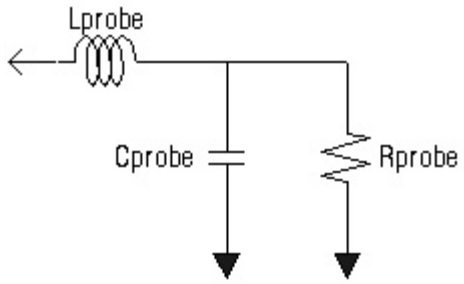

Figure 1. Simplified Load Model of a Logic Analyzer Probe

An important property of a logic analyzer probe is its impedance vs. frequency profile. This gives information to the user about when the impedance of the probe is on the same order of magnitude to the target transmission line impedance. This is important because if the probe impedance becomes too low, it will begin to look like an impedance divider and cause large reflections.

At lower frequencies, the resistor will dominate the probe's impedance and will have minimal effect on the target. This is because the probe impedance is on the order of 20k Ω's and the target is typically 50 – 75 Ω's. The two impedances are in parallel and yield most nearly the target impedance. As the frequency goes up, the probe will begin to look capacitive and its impedance will start to roll off. Once the impedance gets on the order of magnitude of the target impedance, reflections from the probe become an important issue.

At very high frequencies, the probe looks inductive and the impedance will increase. The capacitive and inductive nature of the probe load forms a resonance. The goal of the logic analysis probe is to push its resonance as far up in frequency as possible. In addition, the impedance at resonance should be as high as possible. If the probe impedance gets down in the range of 10-20Ω's, the probe will shunt out the higher frequency components of the target system. Figure 2 shows the equivalent load model of the E5378A, 34 Channel, Single-Ended Probe from Agilent Technologies, Inc. Notice the resistive, capacitive, and inductive components of this model.

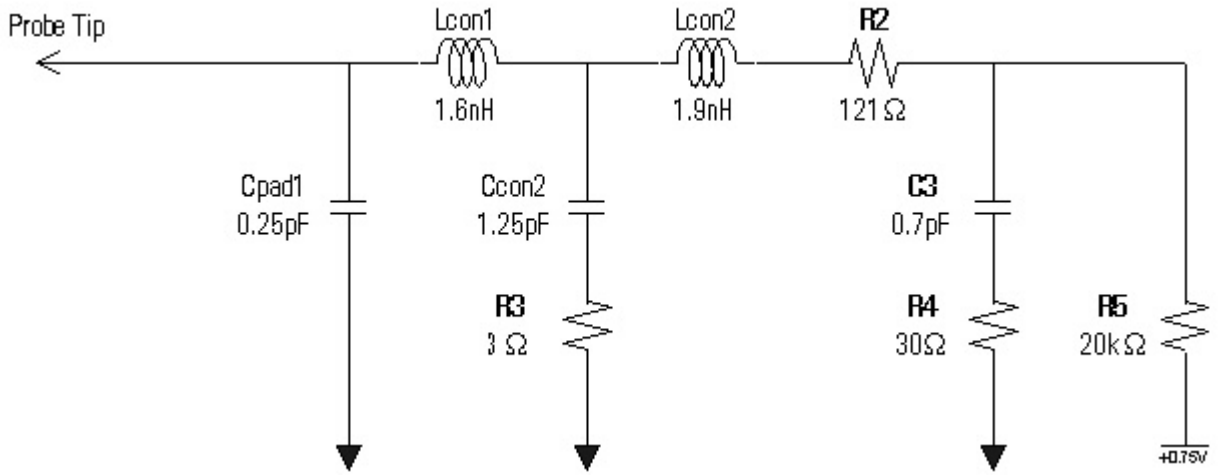

Figure 2. Equivalent Load Model of the E5378A Logic Analyzer Probe

As discussed, simulating the load model is the most accurate method of determining its affect on the system and is always recommended.

For a quick estimate of the probe's affect, a lumped capacitance probe model can be used. Logic Analyzer probe vendors provide a lumped capacitance estimate of each probing form factor. With the equivalent lumped capacitance, a time constant is formed with either the termination resistance or the impedance of the transmission line. This equivalent τ can then be used in an RMS sum of the time constants in the system. Once the overall system time constant is found, this can be converted to risetime and bandwidth to predict the contribution of the probe to the overall performance of the system.

Another interesting characteristic of an analyzer probe is its impedance profile. The effect of a logic analyzer probe on a target is characterized by performing multiple high-frequency measurements. These measurements include Voltage Network Analyzer (VNA), Time Domain Reflectometry (TDR), and Time Domain Transmission (TDT). These measurements are taken on a near perfect 50 Ω system that is double-terminated. Using a near perfect system isolates the effect of the probe from the effect of the test fixture. A logic analyzer vendor will create an RLC model (shown in figure 2) that accurately models the measurements. The RLC model can then be used in simulations as an accurate representation of the probe. Figure 3 shows the impedance response of the E5378A Logic Analyzer Probe from Agilent Technologies, Inc. Notice at low frequencies, the probe has a high impedance (20k Ω's). As the frequency increases, the impedance starts to roll off due to the capacitance of the probe. A resonance occurs at 3.4 GHz at which the impedance is 10 Ω's. Above the resonant frequency, the probe looks inductive and the impedance begins to increase.

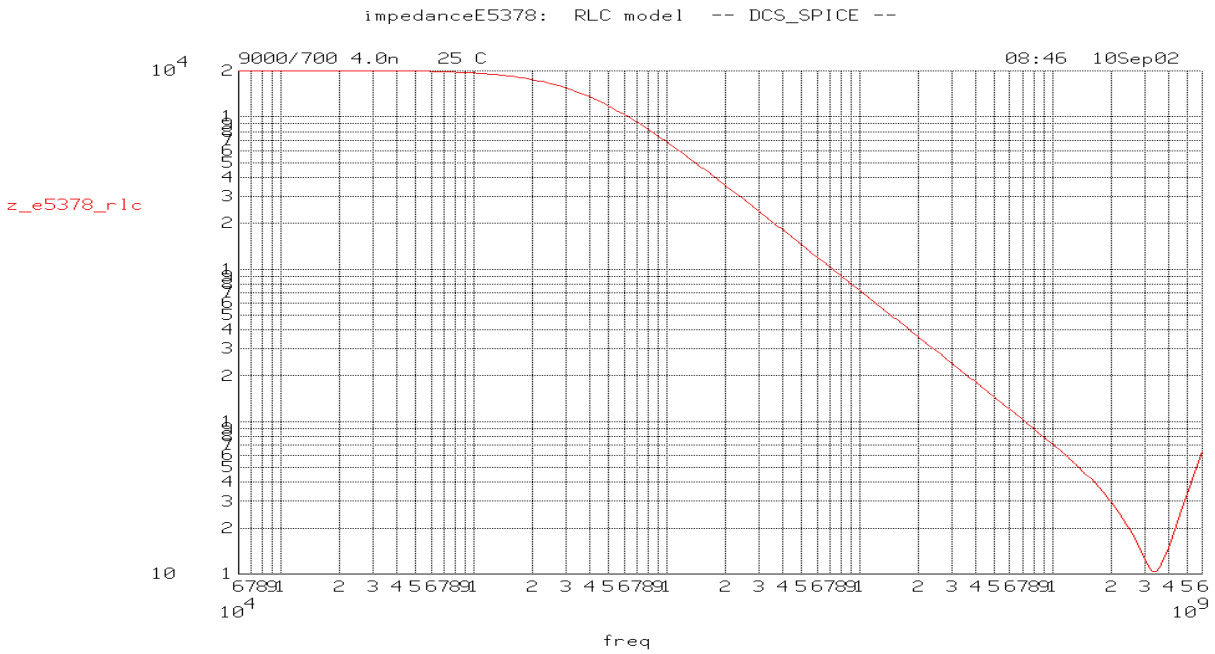

Figure 3. Impedance Response for the E5378A Logic Analyzer Probe

The impedance plot can tell the user information about reflections of certain frequency components. Again it is emphasized that the probe is part of the system and the topology of the transmission line is as important as the probe load. For example, large reflections may be tolerable on a double-terminated transmission line while small reflections may break a system that is poorly terminated.

III. The Effect of Probing Location

Since the probe is part of the circuit and the circuit part of the probe, the effects at both points of interest can be predicted (i.e., the receiver and the probe tip). One of the major variables of the probe's impact is its location on the target transmission line. The reflections that the probe causes will be determined by its relative position on the transmission line. Whether or not the reflections are of severe impact depends on the target system (i.e., trace length, termination scheme, voltage margin, etc…). Figure 4 shows a standard transmission line system highlighting the most common locations where a logic analyzer probe is connected.

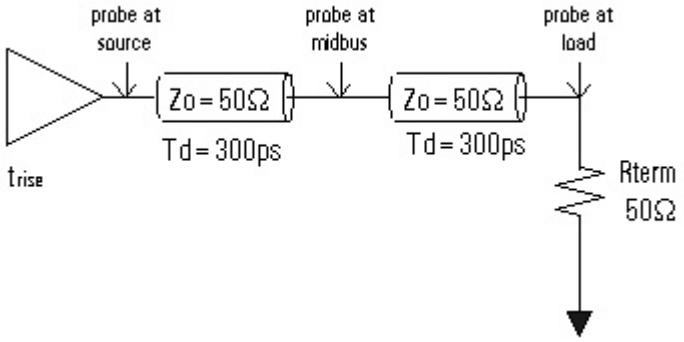

Figure 4. Circuit Topology for a Load-Terminated Transmission Line

LOAD TERMINATED SYSTEM

In a load-terminated system, reflections that are induced are absorbed into the termination resistor at the receiver. If these reflections arrive at the same time as the incident wave or subsequent waves, they manifest themselves as risetime degradation or inter-symbol-interference (ISI). When connecting a logic analyzer probe to the system, the probe will look like a capacitive discontinuity. The best location to insert the probe in this type of system is at the source. The first reason for this is that the reflection off of the probe occurs instantaneously at the driver. This reflection then re-reflects off of the low impedance driver and travels down the transmission line with the incident wave. The received waveform experiences risetime degradation but has minimal secondary reflections. Second, to reduce the effect of the capacitive load on the system, the RC time constant formed by the probe should be as low as possible. The capacitance of the probe cannot be changed however the resistance/impedance of the time constant will depend on the location of the probe. By inserting the probe at the source, the resistance/impedance of the time constant is the parallel combination of the low impedance driver with the transmission line impedance. This combination yields the lowest resistance/impedance in the system and hence the lowest RC time constant.

SOURCE TERMINATED SYSTEM

In a source-terminated system, the incident wave divides in amplitude across the source termination resistance and the impedance of the transmission line. The half amplitude wave travels to the receiver where it experiences a 100% positive reflection. This reflection superimposes itself with the incident wave to yield the original amplitude of the driver. The reverse traveling reflection propagates back to the driver where it is absorbed into the source termination resistor. The architecture of a source-termination is such that at any place on the transmission line besides exactly at the receiver, the waveform observed will have a stair-step shape. A logic analyzer decides whether the signal being

probed is a '1' or a '0' by comparing it with a user defined threshold voltage (typically centered in the voltage swing). This means that if the logic analyzer probe is located anywhere besides directly at the receiver, it will observe this stair-step waveform shape. For the duration of time that the waveform resides in the middle of the swing, the logic analyzer will not be able to determine the logic level. This directly affects the timing performance of the analyzer. For a source-terminated system, the logic analyzer probe should be placed as close to the receiver as possible.

DOUBLE TERMINATED SYSTEM

In a double terminated system, only half of the original signal will reach the receiver due to the resistive divider formed by the source and load termination resistor. The logic analyzer probe can be placed anywhere on this type of system. The main consideration is the RC time constant of the probe. However, at any location on the system, the resistance/impedance will be ½ the characteristic impedance of the line (i.e., 50Ω//50Ω). Since only half of the original voltage level will be observed at the probe tip, the designer must make sure that the logic analyzer *minimum voltage swing* specification is met.

IV. Stub-Probing

Stub probing refers to when the probe tip cannot be placed directly on the target's transmission line. The length of trace that runs between the probe tip and the target signal is called the stub. The stub can consist of PCB trace, wire, or the leads of a connector. Stub probing is difficult to avoid due to layout constraints on a PCB. The question then becomes how close does the probe tip need to be to the transmission line and still have acceptable performance in the system and in the logic analyzer?

When talking about transmission lines, the rules of thumb that are used are applicable to logic analyzer stubs. The rules of thumb depend on the system risetime. For a logic analyzer, the recommendation is that the stub have an electrical length of no more than 20% of the system risetime. For an electrical length that is less that 20% of the system risetime, the stub can be treated as a lumped capacitance and not a distributed transmission line. However, the capacitance increases greatly as the stub length increases. At a point, the trace capacitance will exceed the total capacitance of the probe. The following figure shows the stub-probe topology.

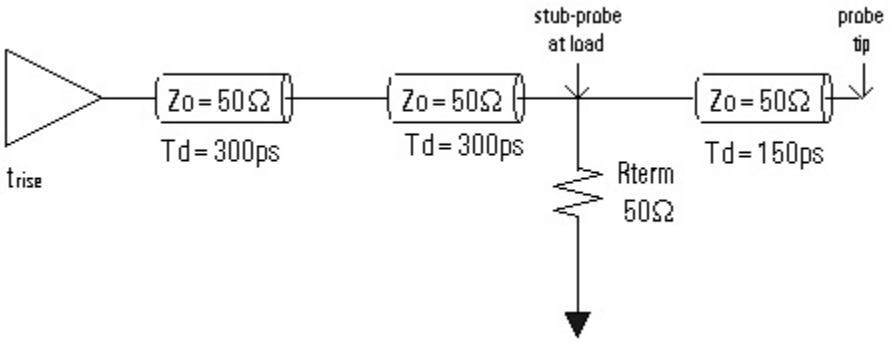

Figure 5. Load-Termination Topology with Stub-Probe at Load

The following example illustrates the maximum stub length acceptable for particular risetimes. This example uses a propagation velocity of 150ps/in, which is typical in FR4 dielectric PCBs. The unit capacitance is typically 3pF per inch for a standard 50 Ω, FR4 microstrip transmission line

Example:

Trise= 150ps,	Tstub=(150)*(0.2)= 30ps	Length=(30)/(150)=0.20”	Cstub=(0.2)*(3p)=0.6pF
Trise= 250ps,	Tstub=(250)*(0.2)= 50ps	Length=(50)/(150)=0.33”	Cstub=(0.33)*(3p)=1.0pF
Trise= 500ps,	Tstub=(500)*(0.2)= 100ps	Length=(100)/(1500)=0.67”	Cstub=(0.67)*(3p)=2.0 pF
Trise= 1000ps,	Tstub=(1000)*(0.2)= 200ps	Length=(200)/(150)=1.33”	Cstub=(1.33)*(3p)=4.0pF

If we look at a logic analyzer probe that is connected though a 1” stub to the load of a transmission line, we can illustrate the above example. The following figures show the effect of a 1” stub-probe on a load-terminated transmission line when probed at the load. Four risetimes are presented. The 150ps, 250ps, and 500ps risetimes consider the 1” stub to be unacceptable while the 1000ps risetime will operate properly. It is obvious from this figure that the 1000ps risetime has considerably better characteristics than the 150ps risetime.

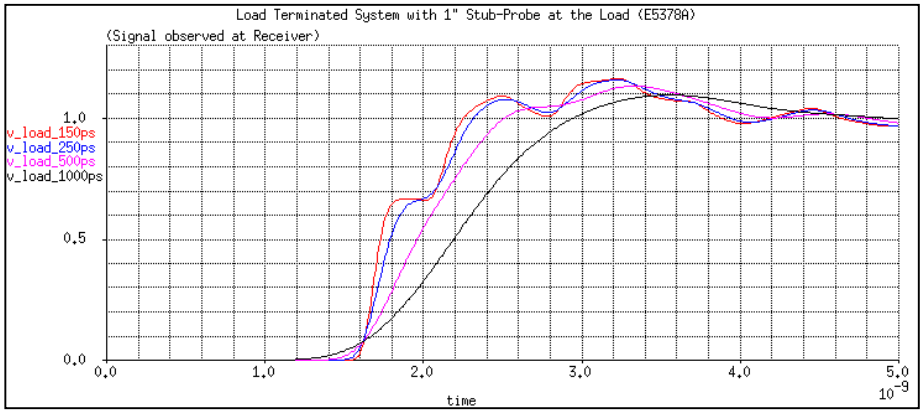

Figure 6. Signal at Receiver of Load-Terminated System with 1” Stub-Probe at Load

The next figure shows the signal at the probe tip for a 1” stub-probe. Again it is obvious that the 1000ps risetime has better characteristics than the 150ps risetime.

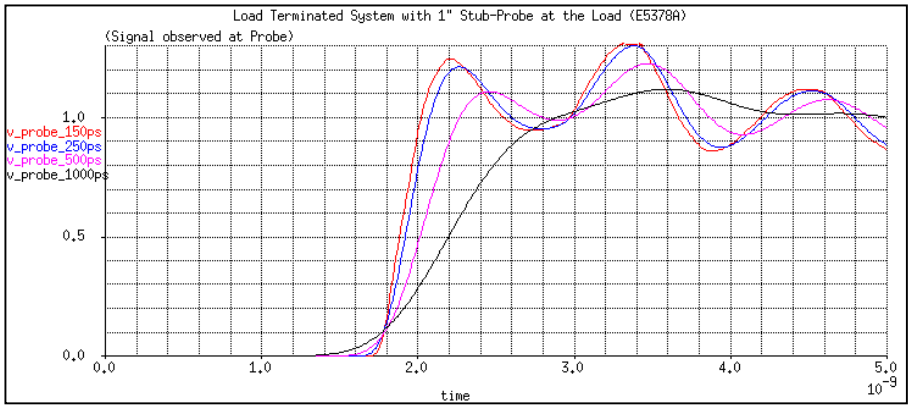

Figure 7. Signal at Probe Tip of Load-Terminated System with 1” Stub-Probe at Load

Another perspective of the effect of stub probing is to view the same system risetime at different stub lengths to the probe tip. The system will experience difference responses due to the stub changing from a lumped capacitive load to a distributed stub load. The probe tip will experience more severe ringing as the stub length increases. The following figures show the effect of a 500ps system risetime in a load terminated transmission line with the probe tip connected at the load. The distance between the probe tip and the transmission line varies from 0" to 2" in 0.5" increments. The first figure shows the waveform as observed by the receiver. The second figure shows the waveform as observed at the probe tip. These figures show the waveforms for an extended time period of 10ns. This is to emphasize how long the reflections stay in the system as the stub-length increases. For the 2" stub length case (2"), there is still substantial ringing at the probe tip occurring up to 8ns after the initial edge.

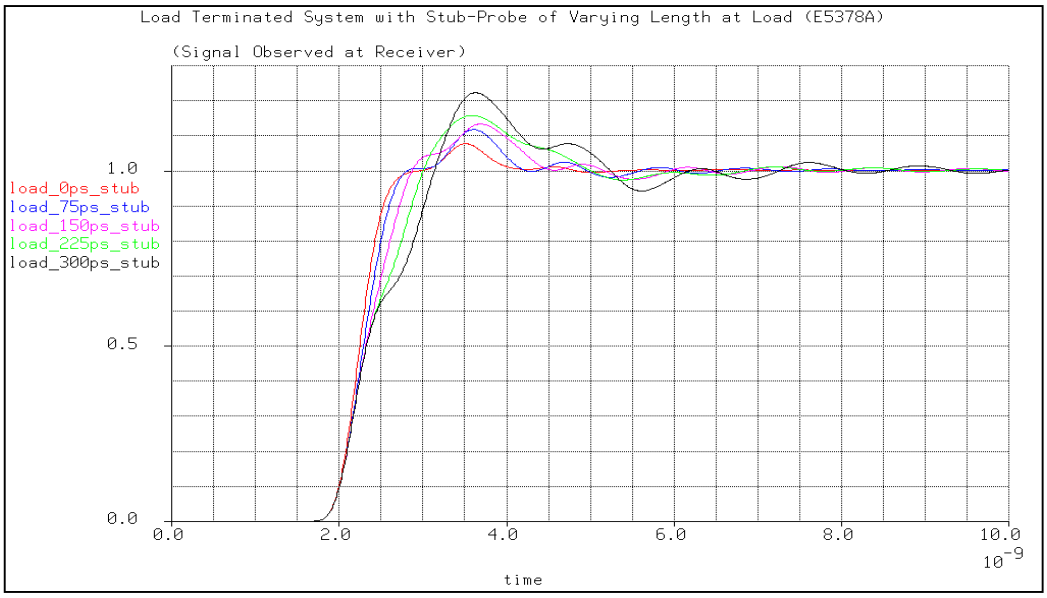

Figure 8. Signal at Receiver of a Load-Terminated System with a Varying Stub-Probe at Load

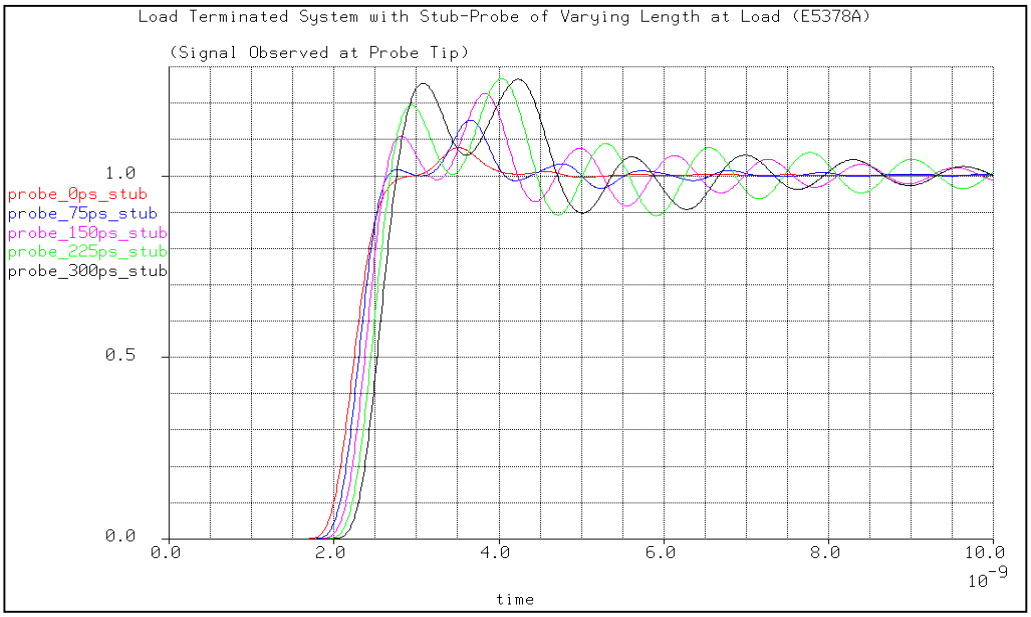

Figure 9. Signal at Probe Tip of a Load-Terminated System with a Varying Stub-Probe at Load

Clearly the addition of transmission line stub between the probe tip and the probed system can severely affect the signal quality at both the receiver of the target and at the probe tip of the logic analyzer. One way to improve the performance of the probe and system when the probe tip cannot be placed directly on the target system is a method called "damped resistor probing". By inserting a damping resistor directly at the target, a longer stretch of stub can be tolerated to the probe tip. The damped resistor serves two purposes. First, it isolates the target system from the capacitive loading of the stub-probe. In addition, it dissipates the energy of the reflections. The next figure shows the topology of the damped-resistor probing scheme.

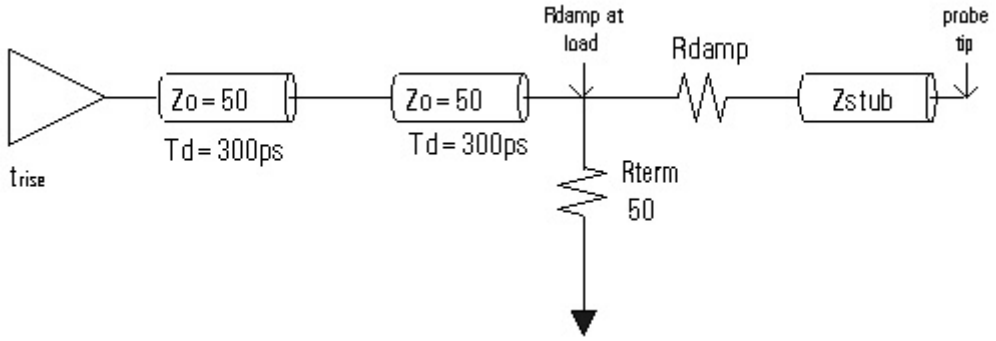

Figure 10. Load-Termination Topology with Damped Resistor Probe at Load

To illustrate the importance of minimizing the stub length, consider the following example. The Agilent Technologies' E5387A Soft Touch Logic Analyzer Probe is connected to a load terminated system through 0.5" of stub length. Using the signal integrity tool "Eye Scan", the eye diagram of the probed signal can by mapped. The next figure shows the eye diagram of the signal at the logic analyzer probe tip as seen by Eye Scan. The probed waveform is a 500Mb/s, 400mVpp signal.

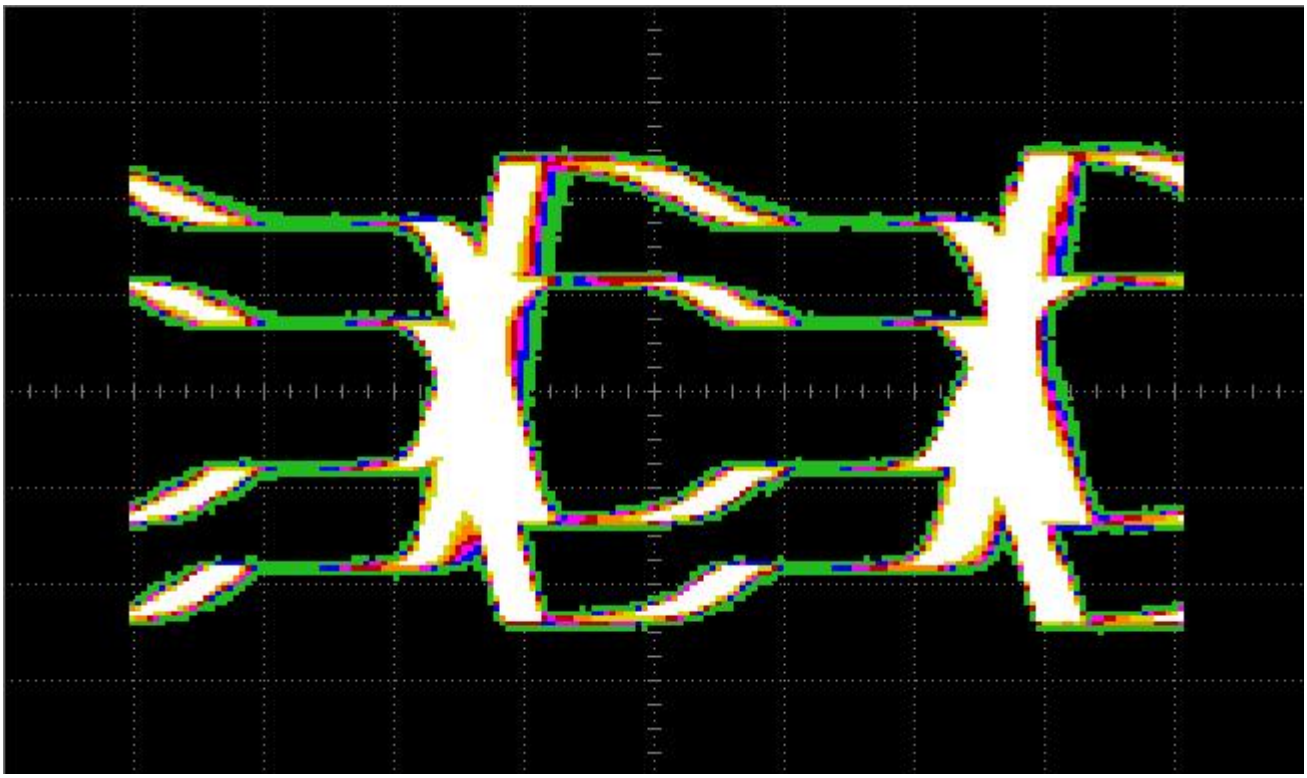

Figure 11. Eye Scan Diagram of a Signal Probed through 0.5" of Stub

The next figure shows the same signal being probed with the E5387A, but in this case a 125Ω damping resistor is placed at the target to isolate the target and damp oscillations.

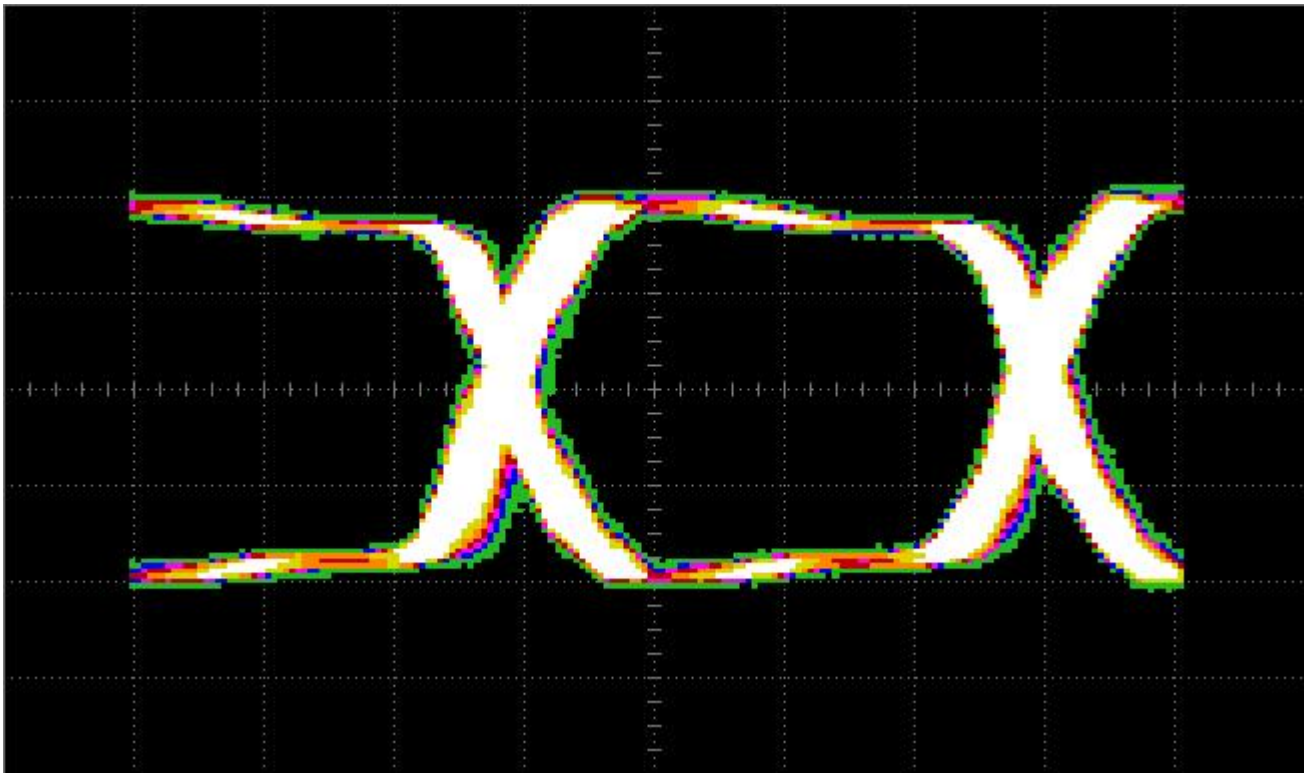

Figure 12. Eye Scan Diagram of a Signal Probed through 0.5" of Stub with 125Ω Damping Resistor

These Eye Diagrams clearly show the impact of a damping resistor on the signal that the Logic Analyzer sees. In one instance, the signal is nearly unusable to the logic analyzer. By simply inserting a damping resistor, the signal quality improves to the point where the load of the logic analyzer probe is negligible.

Probing techniques are even more important in modern logic analyzers that contain signal integrity tools such as "Eye Scan" by Agilent Technologies. Logic Analyzer are providing analog insight into the behavior of the signals being probed. In order for this analog information to be of any use, the probe itself must not distort the waveform being displayed. If the probe loading can be minimized, then the Eye Diagrams that are produced can be accepted as a true analog representation of what is happening in the system. This becomes a very powerful tool to debug signal integrity problems. The main advantage of logic analyzer signal integrity tools is the ability to take analog measurements across many channels simultaneously. As many as 340 signals can be observed using Eye Scan with the latest suite of logic analyzer modules from Agilent Technologies (16753A, 54A, 55A, and 56A). These new tools bring a whole new perspective into signal integrity and system debug. However, as shown in the previous figures the probing is critical to the success of the measurement.

There are many form factors of probes that enable the user to make a successful connection to the target and avoid these signal integrity problems. The next section shows some of the available probing form factors for modern logic analyzers.

V. Modern Probing Solutions

The mechanical considerations of a logic analyzer probe are just as important as the electrical ones. If the form factor of the probe does not easily integrate itself into the target system, then the probe is not useful. As discussed in previous sections, probe location makes a big difference to the signal integrity of the system and of the logic analyzer. The size and shape of the probe play a part in how close the probe tip can be placed to the target transmission line.

Logic analyzer probing solutions have evolved into four main categories:

1) Connector-Based - mating connectors between the target and the probe
2) Connector-Less - only landing pads on the PCB
3) Flying Lead Based - individual probe cable for each signal
4) Custom - application specific probing

The following figure shows a picture of each of the first three probing solutions previously described. On the left is the "E5378A, 34 Channel, Single-Ended Samtec probe". In the middle is the "E5382A, 17 Channel, Single-Ended Flying Lead probe". On the far right is the E5387A, 17 Channel, Differential Soft Touch (connector-less) probe. All of the probes shown are from Agilent Technologies, Inc.

Figure 13. Modern Probing Solutions
(Connector-Based, Flying Lead, and Connector-Less)

MEMORY SYSTEM PROBING

There are two probing solutions that are very well suited to memory system verification, the connector-less and custom logic analyzer probes. The connector-less probe connects to the target through the use of landing pads on the PCB and a spring-pin technology on the probe. What makes this probing solution so appealing is the flow-through routing capability of the pinout. The following figure shows the routing diagram of the E5390A, 34 Channel, Single-Ended, Connector-less Probe from Agilent Technologies.

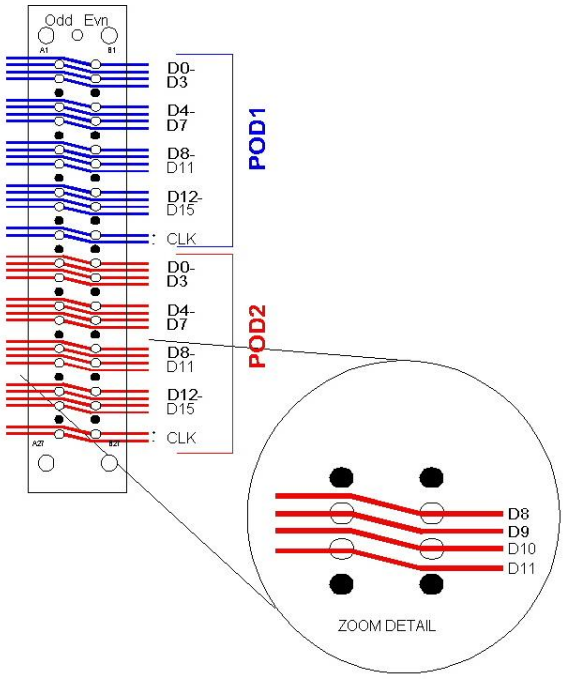

Figure 14. Flow Through Routing of the E5390A Connector-Less Probe

This type of probe lends itself well to embedded memory system debug. With this type routing capability, the lines of the memory system can be brought out to logic analyzer testpoints without disturbing the routing flow. In addition, the low loading of these new connector-less probes (0.7pF) means that the system will operate with minimal affect from the probe connection.

The second type of probe form factor that is very useful to memory system debug are custom solutions. There are a variety of custom memory solutions available that solve the mechanical challenges of probing for the designer. The following figure shows the FS2330 probe from FuturePlus Systems. This probe is designed to probe DDR266, socketed memory systems.

Figure 15. Custom Logic Analyzer Probe for DDR266 from FuturePlus Systems

Another custom logic analyzer probe for socketed memory is the FS2331 probe from Future Plus Systems. This probe is designed to probe DDR333 memory systems.

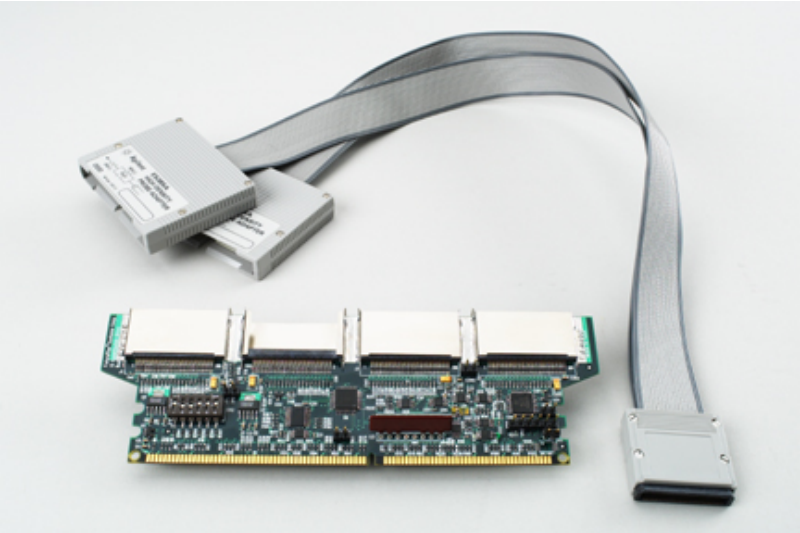

Figure 16. Custom Logic Analyzer Probe for DDR333 from FuturePlus Systems

All of these form factors allow the designer to verify his memory design at the system level in its native environment. Again it is stressed that no matter the form factor, the electrical loading of the probe on the system still needs to be considered. In addition, the signal quality at the probe tip of the logic analyzer probe needs to be considered.

VI. Conclusion

This paper has presented considerations for successful logic analyzer probing of high-speed digital systems. It was shown that the probe presents a load on the target that depends on the intrinsic load of the probe in addition to the location of the probe on the transmission line. It was also shown that the topology and parasitics of the target will degrade the signal integrity observed at the probe tip. Both of these matters should be considered when using logic analysis.

The topic of *Stub Probing* was then presented as the most common signal integrity issue when using a logic analyzer. The technique of inserting a *Damping Resistor* was given as a way to improve the performance of the system and the logic analyzer when the probe tip cannot be placed directly on the target signal.

Finally, modern probing solutions where presented with an emphasis on memory system debug. The new connector-less probes from Agilent Technologies were shown to easily be integrated into embedded memory designs due to the probes flow-through routing. Custom probing solutions where also presented. These custom solutions were application specific to socketed DDR266 and DDR33 designs.

Logic Analysis is a powerful tool to assist engineers in bringing their products to market. The advantages of logic analysis are well suited for memory system debug due to the insight given within the native environment of the memory components. While the theory of testability is sound, the probing connection lays the foundation for the success of the measurement and hence the success of the system.