[Design View / Design Solution]

Taking Logic-Analyzer Probing For Granted Can Spell Trouble

Your sophisticated logic analyzer will be useless unless you pay attention to the basics: probe form factor, loading, signal quality, and where to probe.

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DESIGN VIEW is the summary of the complete *DESIGN SOLUTION* contributed article, which begins on Page 2.

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For decades, engineers have relied on logic analysis as their main system-validation tool. Thanks to technology advances, the digital systems they design continue to jump in speed and complexity, requiring more sophisticated analysis tools. Logic-analyzer vendors have kept pace with industry demands in terms of speed and functionality. However, in many cases, the physical connection (i.e., the probe) from the analyzer to the target system can cause a performance bottleneck. If the signals received by the logic analyzer are degraded, then the powerful triggering and analysis tools within the analyzer become useless.

The first consideration a designer must make when using a logic analyzer is to decide on the type of probing form factor. Probing connections come in two classes: "designed-in" and "after-the-fact." A designed-in probe has probing test points incorporated into the initial design, such as a connector-based or connectorless probe. An after-the-fact probe refers to systems in which testability isn't incorporated into the design. Rather, the connection is done with an individual probe tip that includes various interconnect accessories. One such example is the "flying-lead" probe.

Other issues designers must consider to achieve a successful logic-analyzer-probing connection include probe loading and signal quality. The article also delves into common problems associated with grounding (e.g., a ground lead that's too long; self-inductance of the ground loop) and presents preventative measures.

Finally, discussion surrounds two common problems that designers run into when using the wrong probing solution: probing at the wrong line location and choosing the wrong interconnect.

HIGHLIGHTS:

Probe Loading	The goal of any probe is to present the smallest possible electrical load to the system. To avoid signal-quality degradation, designers must understand the probe construction.
Signal Quality At The Probe	Signal quality at the probe tip is important because it can cause false negatives in the logic analyzer. Probe location is a key factor, particularly when probing various termination schemes.
Grounding	The ground signal for the probe supplies the reference that's in relationship to the observed signal. The goal of grounding is to supply a return path (or ground connection) that has the lowest possible impedance.

Wrong Probing Solutions	Two common pitfalls plague designers when using the wrong probing solution. One involves probing at the wrong location on the line. For instance, probing a series-terminated system at the driver produces an unwanted stair-stepped waveform at the probe tip. The other pitfall is using the wrong interconnect option. In the article example, a Mictor connector-based probe is used, but signals can't be routed directly through it, forcing the connector to the side of the traces.

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For decades, engineers have relied on logic analysis as their main system-validation tool. Thanks to technology advances, the digital systems they design continue to jump in speed and complexity-requiring more sophisticated analysis tools. Logic-analyzer vendors have kept pace with industry demands in terms of speed and functionality. But in many cases, the physical connection (i.e., the probe) from the analyzer to the target system can cause a performance bottleneck. If the signals received by the logic analyzer are degraded, then the powerful triggering and analysis tools within the analyzer become useless. We'll look at the basic issues that engineers need to know to achieve a successful logic-analyzer-probing connection.

Probing Form Factor

The first consideration a designer must make when using a logic analyzer is to decide on the type of probing form factor. Probing connections come in two classes: "designed-in" and "after-the-fact." The designed-in logic-analyzer probe is where the probing test points are incorporated into the initial design. An example of this methodology is a connector-based or connectorless probe. In each of these cases, the designer puts down the appropriate pads on the pc board and routes the signals of interest to the pads. The logic-analyzer probe has the appropriate interconnect to mate to these contacts. For a connector-based probe, the probe contains the opposite sexed connector as the target. For a connectorless probe, the probe has the compression interconnect that will contact the pads on the pc board.

The after-the-fact probe refers to systems in which testability isn't incorporated into the design. Instead, the connection is achieved using an individual probe tip that includes various interconnect accessories (solder, grabber, and so forth). The most common type of after-the-fact probing is to use a "flying-lead" probe.

Probe Loading

The goal of any probe is to present the smallest possible electrical load to the system. If the probe alters the system's performance too drastically, the probe doesn't help the designer validate the system because the failure may be entirely due to the probe. Loading has two major impacts. First, it degrades the signal quality on the target pc board, which may lead to system failures. Second, it can degrade the signal quality of the observed waveform entering the logic analyzer. This could create false negatives in the validation. To avoid these problems, designers must understand the probe construction.

A probe typically looks like a high impedance. The probe-tip circuitry consists of a tip resistor on the order of 20 kΩ. At low frequencies, the probe impedance will look like this resistance. As the frequency rises, parasitic capacitance in the probe will start to lower its impedance. The impedance will roll off following a standard RC response. This is of concern to the target system because as the probe impedance begins to approach the system impedance, the voltage divider formed with the probe becomes substantial. A low impedance will absorb the majority of the signal and cause system failure.

Capacitance in the probe is mainly due to the construction of the interconnect. For example, if there's a significantly large connector between the target signal and the tip resistor in the probe, this connector will add a large capacitance to the probe load. Using a smaller connector will decrease capacitance.

The newest types of probes introduced to lower electrical loading are called "connectorless." In a connectorless probe, landing pads are put on the target system. The logic analyzer probe features a compression interconnect that makes electrical contact to the target. By removing the physical connector from the electrical path, a very low capacitance is achieved (see the table). Figure 2 shows the equivalent lumped capacitance for a variety of probing form factors, and the effect of each of these probes on a system with a 150-ps rise time.

Signal Quality At The Probe

As mentioned earlier, the signal quality at the probe tip is important because it can cause false negatives in the logic analyzer. This is a source of much frustration for validation teams because they spend their time debugging a problem that doesn't exist. To avoid this problem, the signal quality at the probe tip must be considered.

In addition to simple capacitive loading of the probe, another key factor is the probe location. This is particularly important

when probing various termination schemes. For certain termination schemes, the signal observed by the receiver may have sufficient signal quality, while the signal observed at any other point on the line may be unacceptable.

To illustrate this point, consider a series-terminated transmission line. The theory of a series termination is that the induced waveform instantaneously divides between the source termination resistor and the characteristic impedance of the line. The half-amplitude wave travels down the line to the receiver. Upon arriving at the receiver, it experiences a 100% positive reflection, which doubles the half-amplitude signal, thus yielding the original waveform's amplitude. The reflection travels in the reverse direction down the line until it's absorbed into the source termination resistor, thus ending the transient response.

While such a scheme presents a nice waveform to the receiver, the waveform has a stair-step shape at any point on the line. But a stair-stepped waveform simply doesn't suit a logic analyzer because during the period that the waveform remains at half amplitude, the logic analyzer can't detect whether it's a logic "1" or logic "0". Figure 3 shows the waveforms for this situation. Note that the waveform at the receiver has high signal quality, while the observed waveform at the probe tip is unacceptable. As signal speeds increase, the signal quality at the probe tip becomes important to the success of the measurement.

Grounding

Insufficient grounding is another pitfall that designers fall into when doing logic analysis. The ground signal for the probe supplies the reference that's in relationship to the observed signal. For current to flow and a signal to develop, an electrical signal must always have a return current path. The return path is most always considered to be an ideal conductor with zero resistance. When this isn't the case, voltage will develop across the impedance in the ground-return path. Such voltage will detract from the signal amplitude seen by the logic analyzer. The goal of grounding is to supply a return path (or ground connection) that has the lowest-possible impedance. This allows the analyzer to observe the original signal amplitude.

One common grounding problem is a ground lead that's too long. The long ground lead will have series resistance that can cause a voltage to develop across it. To prevent this problem, the ground lead should not be significantly longer than the signal lead. This will match up the parasitic resistance in both the signal and ground path.

Another common problem when probing is self-inductance of the ground loop. When a loop is formed by the ground and signal leads, a self-inductance will form in the ground path that's proportional to the loop area. This inductance will degrade the system bandwidth due to the inductor's frequency-dependant impedance. At high frequencies, the inductance will prevent charge from traveling through the ground lead, thus reducing bandwidth.

To reduce the problem, designers should try to keep their ground loops as small as possible. This is usually predefined when using a connector-based or connectorless probe. However, with flying-lead probes, there are instances where normal wires will be used to connect the probe to the system. In this case, large ground loops can be formed. To avoid these loops, twist the ground and signal wires together to form a twisted pair. Most flying-lead probes come with connection accessories that assist in this problem.

One other situation that arises when probing is if an insufficient number of grounds are employed. In some probing configurations (such as the flying-lead probe), the user sets the number of grounds. To understand this problem, consider a flying-lead set with 16 signals using only one ground connection. In this situation, the return current for all 16 signals must travel through the single ground connection. The self-inductance of the ground lead is low enough to prevent development of a voltage across it when one or two signals return. But with 16 signals, the current becomes large enough whereby the developed voltage is noticeable.

Solving this problem requires increasing the number of grounds. Ideally, there will be one ground for each signal. The number of grounds needed is proportional to frequency. But the recommendation is to never use more than two signals for one ground. If a user experiences problems capturing correct data with a logic analyzer, this would be one of the first things to check.

With all of the probing options available today, it's sometimes hard deciding on the connection scheme that will ensure success. In some cases, it's even hard to know which solutions are available. The following cases show two common pitfalls that designers may run into when using the wrong probing solution.

Probing At The Wrong Location On The Line

Consider the series-terminated system described earlier. The system is implemented with a driver IC on a backplane card and a receiver located in a BGA package. The user chooses to probe the system at the pin's backplane connector due to its perceived convenience. However, as already demonstrated, probing a series-terminated system at the driver will produce a

stair-stepped waveform at the probe tip of the logic analyzer. Figure 4a shows the connection scheme and Figure 4b shows the resultant waveform observed by the probe.

This waveform is clearly unacceptable. The solution is to probe directly at the receiver. The closest physical probing point to the BGA package will be the breakout via pads on the bottom side of the pc board. Figure 5a illustrates a new connection scheme that solders the flying lead directly to the breakout vias of the BGA. The resultant signal quality is shown in Figure 5b.

Using The Wrong Interconnect Option

Consider a system in which a logic analyzer observes signals that run between two parts on a pc board. The signals run on the outer layer of the pc board and can't withstand more than a 3.5-pF load before system failure. The designer decides to use a Mictor connector-based probe (E5380A) to observe the signals. Due to the pinout and construction of the connector, signals can't be routed directly through it. This forces the designer to place the connector to the side of the traces and add vias to each signal. The connection to the connector is then accomplished using another pc-board layer that runs traces perpendicular to the original signals. Figure 6 shows the routing diagram for such a connection.

Now consider an alternative solution using the E5390A SoftTouch connectorless probe. In this case, the signals can be routed directly through the landing pads of the probe points (Fig. 7). This means that no additional trace capacitance is added to the system. The probe's net capacitance is 0.7 pF. By using this type of connection scheme, logic analysis can be added without causing system failure.

Figure 6

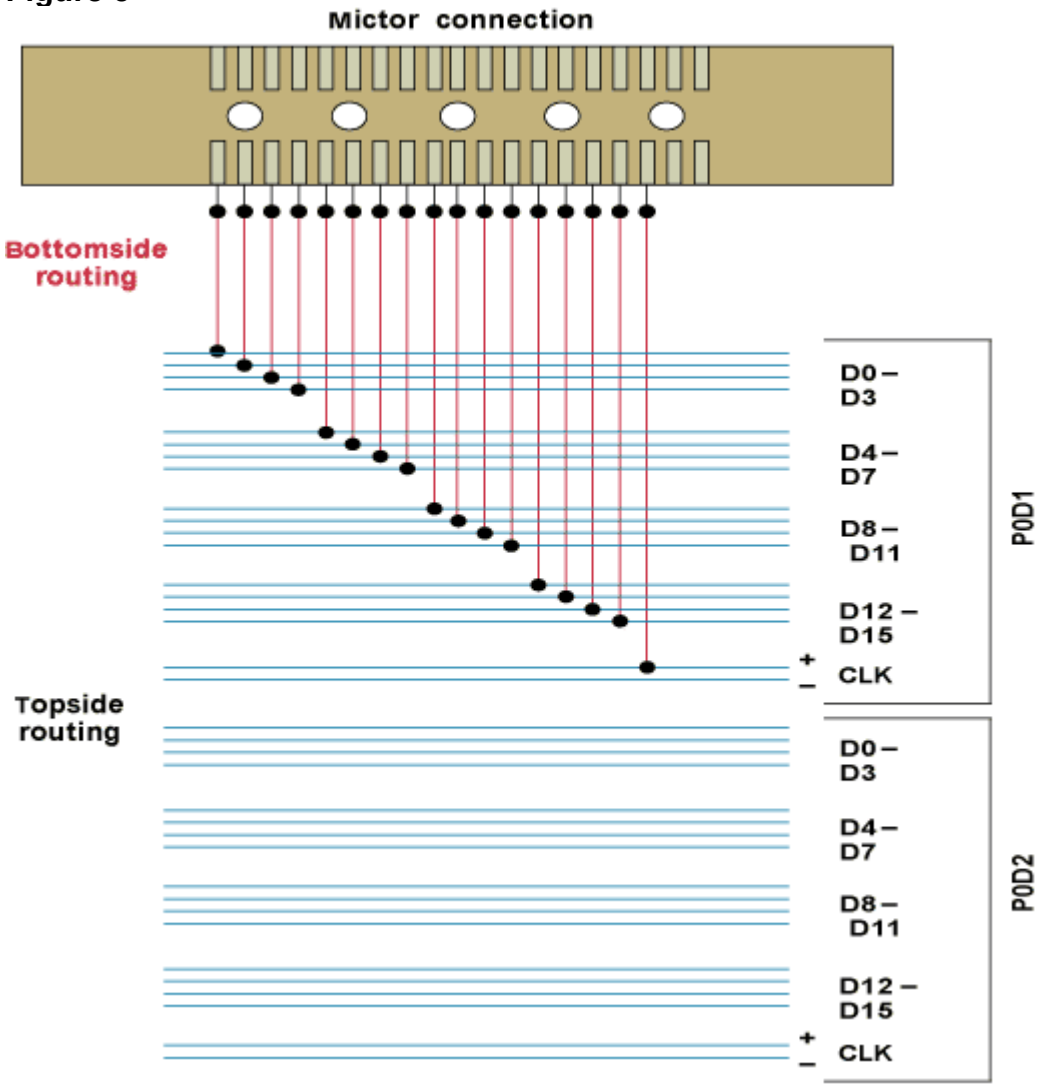

Figure 7